IF-BAND MMICS FOR HIGH-SPEED WIRELESS SIGNAL PROCESSING

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ABSTRACT

IF-band MMICs for high-speed wireless signal processing are presented. The first is a miniaturized 90° divider/combiner with 2.1-dB mean transmission loss for dividing signals at 140 MHz. The second is a logarithmic/limiting amplifier which utilizes a self-phase-distortion compensation technique. More than 65-dB gain and less than 5° phase deviation were obtained.

INTRODUCTION

High-speed wireless communication systems, such as wireless Local Area Networks (LANs), have been attracting a great deal of attention in recent years because they can offer wide bandwidth for achieving the high bit-rates and large capacity needed in the multimedia age. An example of a schematic of the intermediate frequency (IF) part of these systems is shown in Fig. 1. This arrangement requires a logarithmic/limiting amplifier with a Received Signal Strength Indicator (RSSI) to detect the level of the burst signals and interference. Furthermore, a combination of a 90° hybrid and a switch for switching from signal transmission to signal reception is used. In this case, an IF 90° hybrid is fabricated outside the MMIC chip.

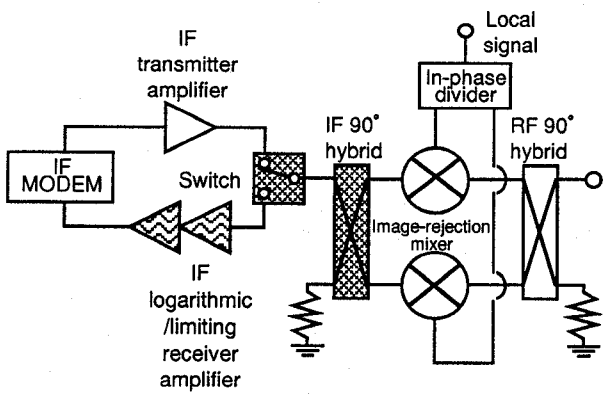

Fig. 1 Example of a schematic of the IF part of the high-speed wireless communication systems.

This paper presents an MMIC 90° signal divider/combiner, which can isolate the transmitted and received signals without using the switch. This leads to the miniaturization of the circuit. Next, an MMIC logarithmic/limiting amplifier with low phase distortion is presented. Low phase distortion is needed to maintain good-quality, high-speed data transmission of signals. Good self-phase distortion compensation is obtained in this amplifier through the use of a combination of a Common-Source FET (CSF) and a Common-Gate FET (CGF) or a combination of a CSF and a Common-Drain FET (CDF).

MMIC 90° DIVIDER/COMBINER

The circuit configuration of a divider with a constant phase difference of 90° is shown in Fig. 2. This divider comprises parallel-connected differential and integral circuits, each of which has a capacitor C and a resistor R. If the impedance levels of ports 1, 2 and 3 are R_{01}, R_{02}, and R_{03}, and R_{02} is equal to R_{03}, the transmission coefficients, S_{21}, S_{31}, S_{12}, and S_{13}, are expressed as fol-

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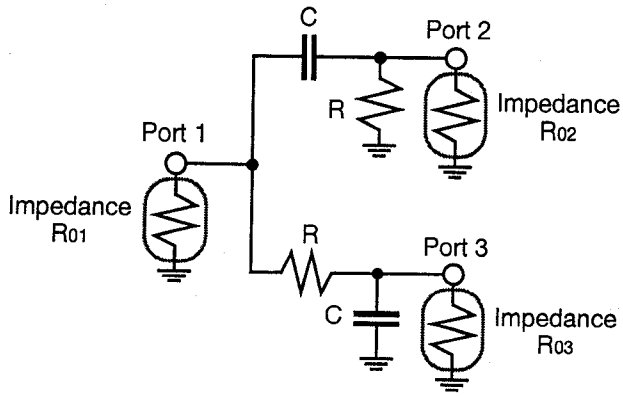


Fig. 2 Divider with a constant phase difference of 90°.

lows:

$$S_{21} = S_{12} = \frac{2\sqrt{R_{01}R_{02}}}{\left(R_{01}+R_{02}+\frac{2R_{01}R_{02}}{R}\right) - j\frac{1}{\omega C}\left(1+\frac{R_{01}+R_{02}}{R}\right)}, \quad (1)$$

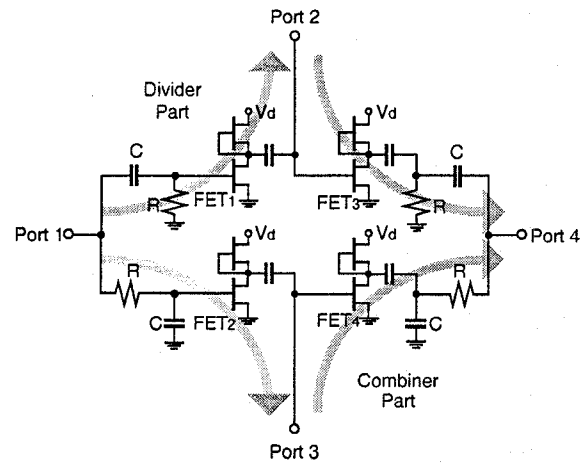
$$S_{31} = S_{13} = \frac{2\sqrt{R_{01}R_{02}}}{\left(R+R_{01}+R_{02}\right) + j\omega C\left\{R\left(R_{01}+R_{02}\right)+2R_{01}R_{02}\right\}}. \quad (2)$$

In general, the condition that 1/(a-jb) is always perpendicular to 1/(c+jd) in the complex plane is

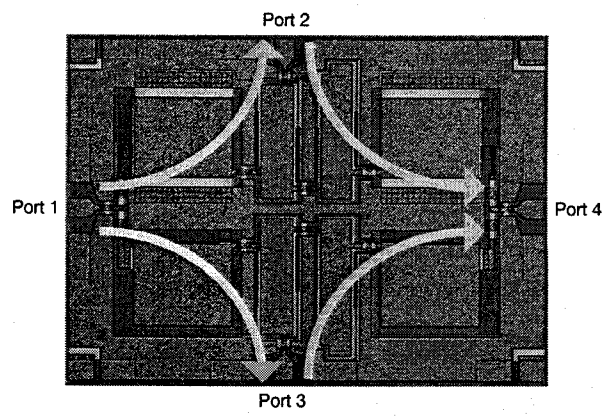
$$ac - bd = 0. \quad (3)$$

Thus the phase difference between $S_{21}(=S_{12})$ and $S_{31}(=S_{13})$ is always 90° at any frequency. Note that the values of R_{02} and R_{03} can be set arbitrarily as long as they are equal to each other. In the previously reported types of 90° phase shifter [1] or 90° combiner [2] using differential and integral circuits, the impedance values of the input and output ports are restricted from the value R.

The configuration of our MMIC 90° signal divider/combiner using GaAs MESFETs [3] is shown in Fig. 3(a). A signal transmitted from port 1 is first divided and then distributed with a phase difference of 90° by the divider part and output with equal amplitude into ports 2 and 3. Leaked signals are amplified by FET_3 and FET_4 and are output into the combiner part. In port 4 of the combiner part, the leaked signals are combined with a phase difference of 90°, and then canceled with equal amplitude and reverse phase. The received signals from port 2 and port 3 are prevented from passing into port 1 by FET_1 and FET_2,



(a) circuit configuration.



(b) photograph of the MMIC chip.

Fig. 3 MMIC 90° divider/combiner.

and thus are output only from port 4.

A photograph of the MMIC chip is shown in Fig. 3(b). The chip size is 1.78 mm x 1.28 mm, which corresponds to less than 1/100 that of the commercial 90° coupler. The gate widths of the GaAs MESFETs are 200 μm.

The amplitude and phase characteristics of the divider part are shown in Fig. 4. The drain voltages are +3 V. The mean transmission loss at 140 MHz is about 2.1 dB, and the amplitude error and phase error are within 1 dB and 3°, respectively, in the frequency range from 130 MHz to 150 MHz. In this frequency range, both of S_{11} and S_{44} are less than -6 dB and S_{41} is suppressed by more than 24 dB.

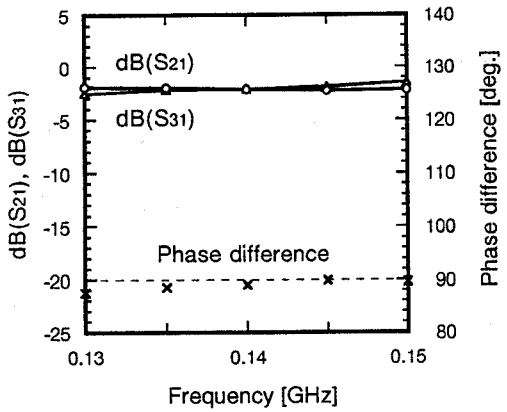


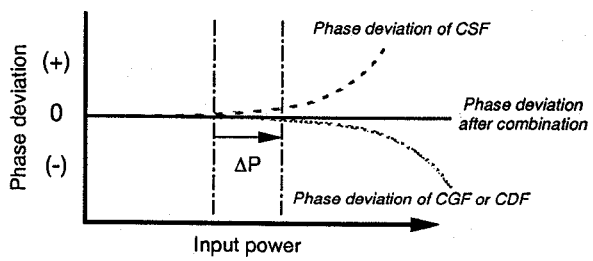
Fig. 4 Measured amplitude and phase characteristics of the divider part.

MMIC LOGARITHMIC/LIMITING AMPLIFIER

We have previously proposed a low-phase distortion technique in which a CSF and a CGF are combined in a power amplifier [4]. The phase distortion compensation can be accomplished in a similar manner by combining the CSF and the CDF. The principle of phase distortion compensation is shown in Fig. 5. The phase distortion compensation can be accomplished by adjusting the bias levels of these FETs.

We designed an MMIC logarithmic/limiting amplifier using GaAs MESFETs by combining a CSF with a CGF at 240 MHz. A block diagram of the amplifier is shown in Fig. 6(a). It employs a successive detection architecture [5].

For the unit amplifier, we adopted a single-ended type amplifier, in which a CGF is cascode-connected with a CSF. The full-wave rectifier is a differential Gilbert type, and the summing circuit has a differential amplifier structure.



(ΔP : Input power level difference caused by CSF gain)

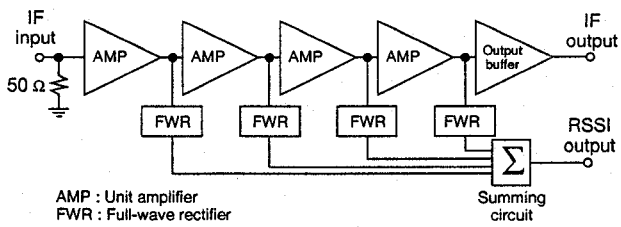
Fig. 5 Phase distortion compensation principle.

A photograph of the fabricated MMIC chip is shown in Fig. 6(b). The chip size is 1.78 mm x 1.78 mm.

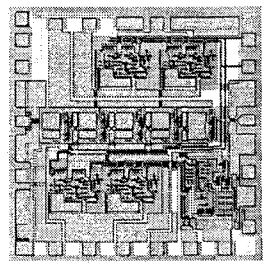
Measured characteristics of the MMIC chip are shown in Fig. 7. The drain and source biases are +3 V and -2 V, and the power consumption is less than 0.24 W. Limiting characteristics are more than 28-dB gain, 3.1-dBm saturated output power and phase deviation of less than 3°. Logarithmic characteristics are 2-dB logarithmic accuracy and RSSI change coefficient of more than 8 mV/dB.

Next, we designed an MMIC logarithmic/limiting amplifier using GaAs MESFETs by combining a CSF with a CDF at 140 MHz. Two MMIC chips are cascade-connected to obtain more than 65-dB gain.

For the unit amplifier, we adopted a single-ended type amplifier, in which a CSF with dc parallel feedback circuit is combined with a CDF [6]. The full-wave rectifier is a differential Gilbert type, and the summing circuit has a differential

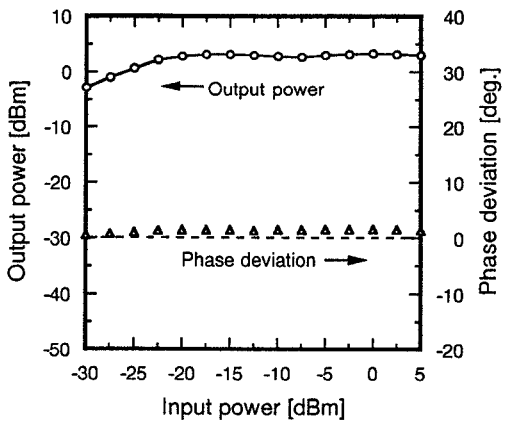


(a) block diagram.

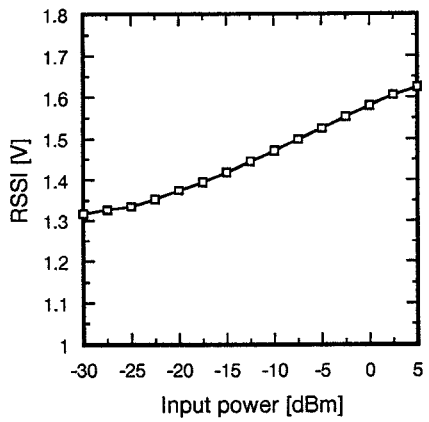


(b) photograph of MMIC chip.

Fig. 6 MMIC logarithmic/limiting receiver amplifier.



(a) output power and phase deviation.



(b) RSSI.

Fig. 7 Measured characteristics of the MMIC logarithmic/limiting receiver amplifier.

amplifier structure. The biases are +3 V and -2 V, and the power consumption is less than 0.58 W. Limiting characteristics of more than 65-dB gain, 2.2-dBm saturated output power and phase deviation of less than 5° are obtained at the input power of -70 dBm to -10 dBm. A logarithmic accuracy of 2 dB and RSSI change coefficient of more than 11 mV/dB are also obtained.

CONCLUSION

IF-band MMICs for high-speed wireless signal processing were proposed. The first is an MMIC 90° divider/combiner with 2.1-dB mean transmission loss for dividing signals at 140 MHz. The second is a logarithmic/limiting amplifier which utilizes a self-phase-distortion compensation technique. More than 65-dB gain and less than 5° phase deviation were obtained.

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REFERENCES

[1] K. Yamamoto et al., "A 1.9-GHz-band GaAs direct-quadrature modulator IC with a phase shifter," *IEEE J. Solid-State circuits*, vol. 28, no. 10, pp. 994-1000, Oct. 1993.

[2] Y. Yamao et al., "Low power quadrature modulator IC's for digital mobile radios," *Proc. 3rd Asia Pacific Microwave Conference*, pp. 771-774, Tokyo, Dec. 1990.

[3] T. Enoki et al., "0.3-μm advanced SAINT FET's having asymmetric n+-layers for ultra-high-frequency GaAs MMIC's," *IEEE Trans. Electron Devices*, vol. 35, pp. 18-24, Jan. 1988.

[4] H. Hayashi et al., "Quasi-linear amplification using the self phase distortion compensation technique," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 11, pp. 2557-2564, Nov.1995.

[5] R. S. Hughes, "Logarithmic Amplification," MA:Artech House, 1986.

[6] N. Ishihara et al., "Gigahertz-band high-gain GaAs monolithic amplifiers using parallel feedback technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 4, pp. 962-968, Aug. 1989.